

## FINAL REPORT

ON

## PROGRAMMABLE PREMODULATION FILTER

FOR

## MANNED SPACECRAFT CENTER

CONTRACT NAS9 6929

SCI W.O. 1767

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Craft, Inc.

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SPACE CRAFT, INC. 8620 SOUTH MEMORIAL PARKWAY HUNTSVILLE, ALABAMA

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#### INTRODUCTION

The purpose of this report is to discuss the objectives and achievements under contract NAS 9-6929 for Programmable Premodulation Filters. The contract was awarded in April 1967 and completed with the submission of this volume in June 1968.

The prime objectives were to design, manufacture and type qualify Programmable Premodulation Filters which meet or exceed the requirements of Exhibit "A" Specification for Programmable Premodulation Filter dated December 1966. Secondary objectives include supplying complete system documentation, reliability documentation and quality assurance documents as required during the term of the contract.

Space Craft has delivered the circuit design breadboard, engineering evaluation unit, Type Qualification Unit and two (2) Flight Qualification Units, which fulfills the requirements of the prime objectives.

Accomplishment of the secondary objectives has been completely successful with documentation submissions on every phase of the program to support results and progress achieved. Space Craft responded to all MSC requests for clarification or additional information required by MSC.

### INITIAL REQUIREMENTS AND MODIFICATIONS

The design requirements are specified in detail in the MSC Exhibit "A" Specification for Programmable Premodulation Filter dated December 12, 1966. The specification outlines the requirements of operation, flexibility, accuracy and reliability for a signal conditioner which accepts a NRZ pulse code wavetrain and filters out undesirable frequencies.

Review of the specification revealed that most of the required parameters were successfully achieved on a contract with identical requirements in most areas. The programming requirement was an additional requirement which is the result of using more than one filter in the circuit and being able to select the desired filter from a remote control position.

The programming circuitry was initially on the same ground system as the signal output circuits, but the specification was amended to provide D. C. isolation between the programming and all other circuits.

The desired filter output characteristic as stated in paragraphs 5. 9. 2. 1 through 5. 9. 2. 1. 4 is not physically attainable. The specification was amended to allow the delivery of a sixth order active filter as proposed in SCI proposal P67-116. A seventh order filter was used to obtain a characteristic which closely approximates the required band pass characteristic and yields a final attenuation in accordance with the specification.

#### DESIGN SUMMARY

The initial design requirements were stated in the MSC Exhibit "A"

Specification for Programmable Premodulation Filter dated December 12,

1966. The stated intent of the specification was to specify the parameters of NRZ pulse signal conditioner. The signal conditioner accepts a NRZ wavetrain and produces an output which passes low frequency signals and rejects frequencies higher than a selected value. The filter is programmable in that the low pass characteristic may be changed from one frequency to another in pre-selected steps with a binary code. The binary code is a combination of ones (3.5V to 10.0V) and zeros (0.0V to 0.5V) arranged in a logical binary form to binary count from one to fourteen. The binary numbers are decoded by the signal conditioner which selects one of the fourteen filters for operation.

The power for the filter is provided from an external source which is 28+ 4 volts. The external source is isolated from the signal input, binary input and signal output by a power converter using a transformer to A. C. couple a chopped D. C. to the circuits requiring power. The signal input, binary input, power input and signal output are totally D. C. isolated with individual windings on the power converter transformer.

The signal input buffer accepts input wavetrain with 4.0 volts to 7.0 volts amplitude and 1.0 microsecond rise and fall times.

The buffer provides a high input impedance and D. C. isolation between the signal input common and the signal output common. The transformer used for signal D. C. isolation differentiates the input waveform and produces a narrow pulse, which occurs at the leading and trailing edges of each input pulse. The narrow pulses are used to toggle a binary element and reconstruct

the input wavetrain.

The binary element is a monolithic circuit with a toggle speed in excess of ten (10) megacycles. The toggle inputs are biased to obtain a toggle threshold voltage between one and two volts. The threshold voltage insures against false triggering from noise or signals below the acceptable limits. The binary element is followed by a stage of gain to provide low output impedance required to drive all fourteen filters simultaneously. All filter inputs are connected directly to the drive stage, thereby reducing the circuit complexity by eliminating fourteen separate switching circuits.

The filter circuits are low pass characteristics defined by a given set of Bessel Polynominals. The filter is a seventh order filter which guarantees the final roll off of 36 db/octave minimum. The final attenuation rate is not obtained until several octaves past the corner frequency. The active elements are two complementary transistors connected with 100% feedback for unity gain. Each filter output is connected to a junction field effect transistor which acts as a signal switch to the output buffer amplifier. The switch is biased normally "off" and is turned "on" with the application of the positive bias which turns the filter "on". The output buffer consists of two independent circuits which are driven from a common point. Both circuits are "cascode doublet" amplifiers. Amplifier number two (2) is a unity gain amplifier with the forward biased diode compensating for Vbe temperature variations of the input transistor. The output is unipolar from ground to five volts peak.

Output number one is a "cascode doublet" with a gain adjustment. The gain and offset is adjusted to obtain a signal balanced about ground. The peak to peak amplitude is adjusted for approximately 8 volts.

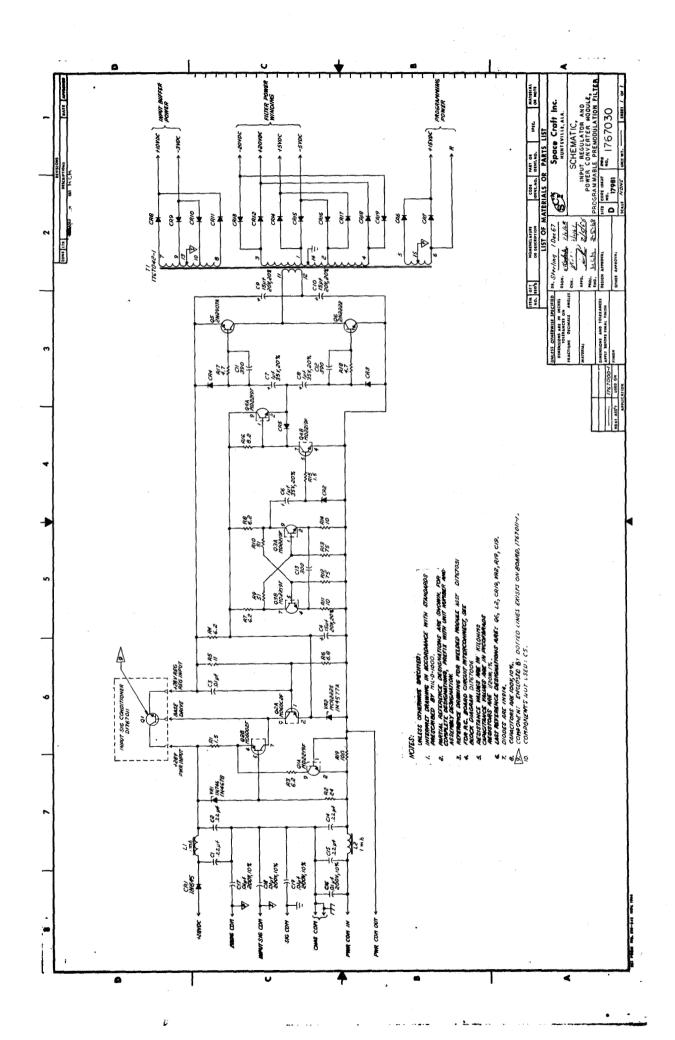
#### CIRCUIT DESIGN

## Power Converter

The schematic of the power converter is shown in figure 1. The functions of the power converter are to provide system power, D. C. isolation, reject line variations and eliminate radio frequency interference. The converter can be divided into five sections which are the input filter, the series regulator, the square wave oscillator, the chopper stage and the power transformer. The input filter consists of a filter and reverse voltage protection. Reverse voltage protection is provided by CR1 to eliminate any possibility of damage in the event the power source polarity is accidentally reversed. The filter components are values chosen to be most effective at higher frequencies.

High frequency attenuation on the input to the power converter is important since stray capacitive coupling increases with increasing frequency. The high frequencies are bypassed to chassis common with ceramic capacitors  $C_1$ ,  $C_2$ ,  $C_{15}$ , and  $C_{14}$ . The inductors  $L_1$  and  $L_2$  are the inductive reactances of the filter. All common lines are coupled to chassis ground with the capacitors in the input filter.

The series regulator is  $Q_1$  with a constant current generator  $V_{r1}$ ,  $R_2$ ,  $R_1$  and  $Q_{2b}$  and a comparator  $Q_{2a}$ . The constant current generator is employed to minimize the effects of input line variations on base current to the series element. The comparator amplifier  $Q_{2a}$  compares a feedback sample produced by  $R_5$  and  $R_6$  with the reference  $V_{r2}$ .  $Q_{2a}$  produces an error signal in proper phase and magnitude to exactly compensate the output voltage.



The square wave generator is a current mode astable multivibrator with  $Q_{3a}$  and  $Q_{3b}$  operating in a non-saturating mode. The current mode circuit was selected over more conventional multivibrators to obtain fast rise and fall times and minimize start up problems. Current mode multivibrators do not experience start difficulties because only one timing capacitor is used with D.C. cross coupling, insuring that both transistors cannot be in the same state at the same time. The fast rise and fall times are achieved by taking the output from the collector of  $Q_{3a}$  where the switching times are independent of the charging current for the timing capacitor. The multivibrator is sensitive to load variations and for that reason is followed by a stage of gain to drive the power stage. The buffer is  $Q_{4a}$  and  $Q_{4b}$  which delivers the base current to the power stage transistors  $Q_5$  and  $Q_6$ . The power stage is connected to switch the power transformer between the regulated 20 volt line and ground through saturated transistor switches.

The power transformer provides the A. C. coupling to the individual circuit loads. The windings are placed on a ferrite toroid core which offers the highest permeability per unit volume available. The primary turns are computed using Faraday's equation  $E = 4NFBA \times 10^{-8}$  where E is the applied voltage, N is the number of turns, F is the frequency of oscillation, B is the maximum flux density at saturation and A is the cross sectional core area. The secondary turns are computed from the voltage ratio desired and the primary turns. The diodes on the secondary windings restore the A. C. to D. C.

The power converter uses the same basic approach as the design proposed by SCI in proposal P67-116. The detail circuitry is more sophisticated to improve the high frequency attenuation on the input lines, the low frequency rejection has been improved. The addition of the current limiter Q<sub>1a</sub> to

protect the system against excessive current under short circuit conditions and additional windings for the required D. C. isolation further increases the complexity of the power converter.

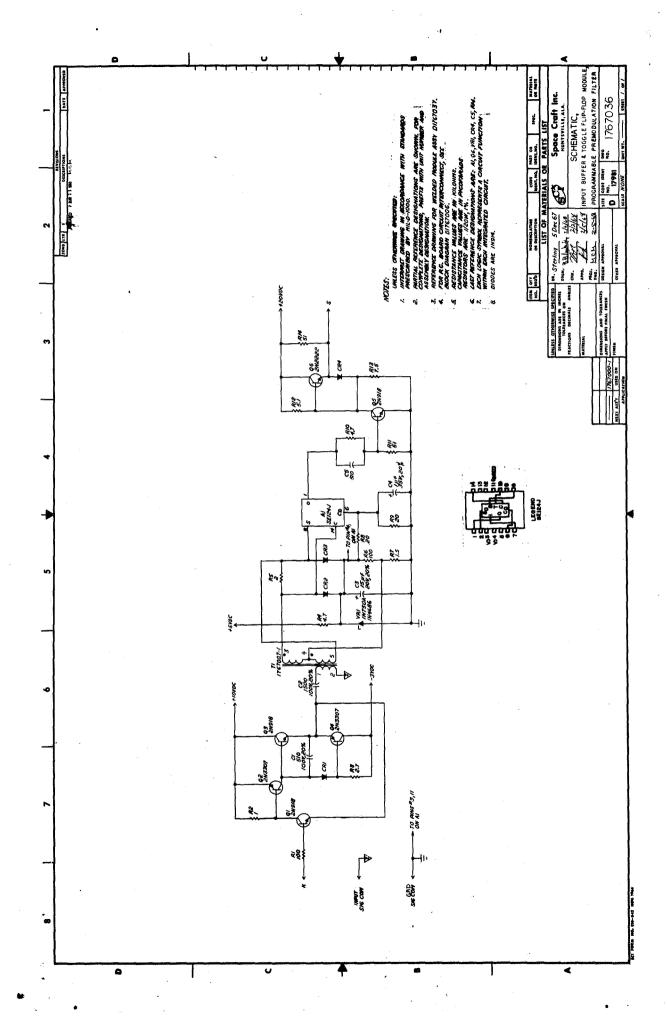
#### Input Signal Buffer

The input signal buffer shown in Figure 1767036 is identical to the circuit used on the previous contract. The component values were changed to obtain the high frequency response required in the present specification.

The previous buffer was required to operate to a frequency less than 10 KC, whereas the present requirement is for 50 KC minimum.

The component values were thus chosen to yield a frequency response greater than 300 KC. The input impedance remains greater than 500 K, with overvoltage protection to 33 volts minimum. The buffer operates closed loop as a unity gain non-inverting amplifier, with a differentiation network composed of  $C_2$  and  $T_1$ . The differentiation is important in that the leading and trailing edges produce narrow pulses which define the period of the input waveform for a toggle flip-flop. The toggle flip-flop reconstructs the input waveform from these pulses.

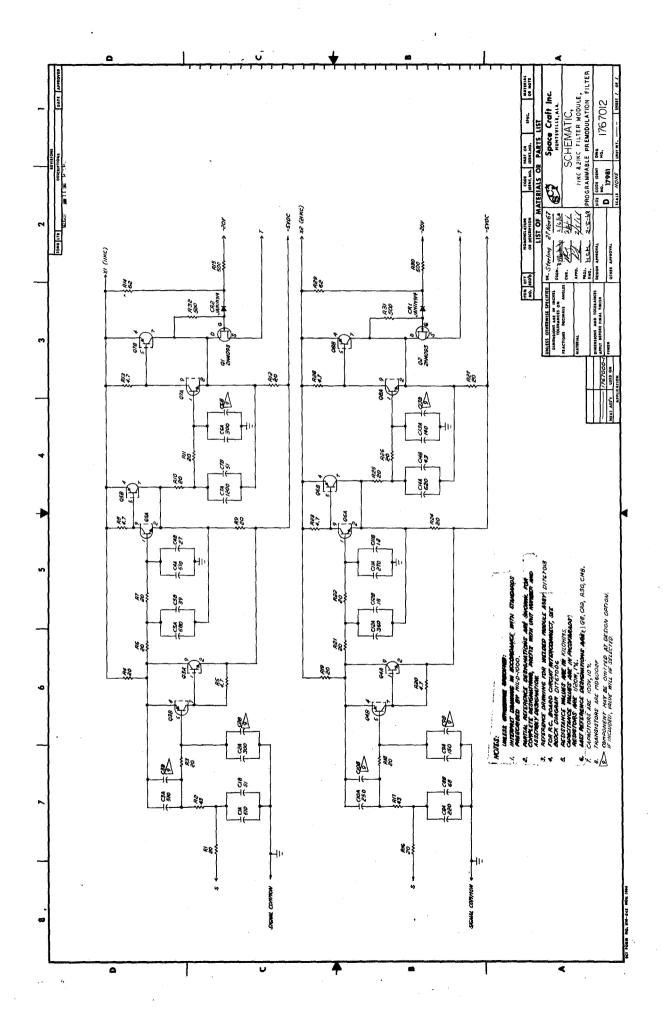
The flip-flop is an integrated circuit with a toggle response greater than 10 MHZ. The change to the integrated circuit was made to gain the higher frequency response required in the present design. The flip-flop drive circuit is biased to a positive voltage to provide noise rejection of one to two volts. The integrated circuit also yields greater reliability since the total number of components is reduced. The output of the binary element is a buffer with a stage of gain to drive the load presented by the fourteen filters.

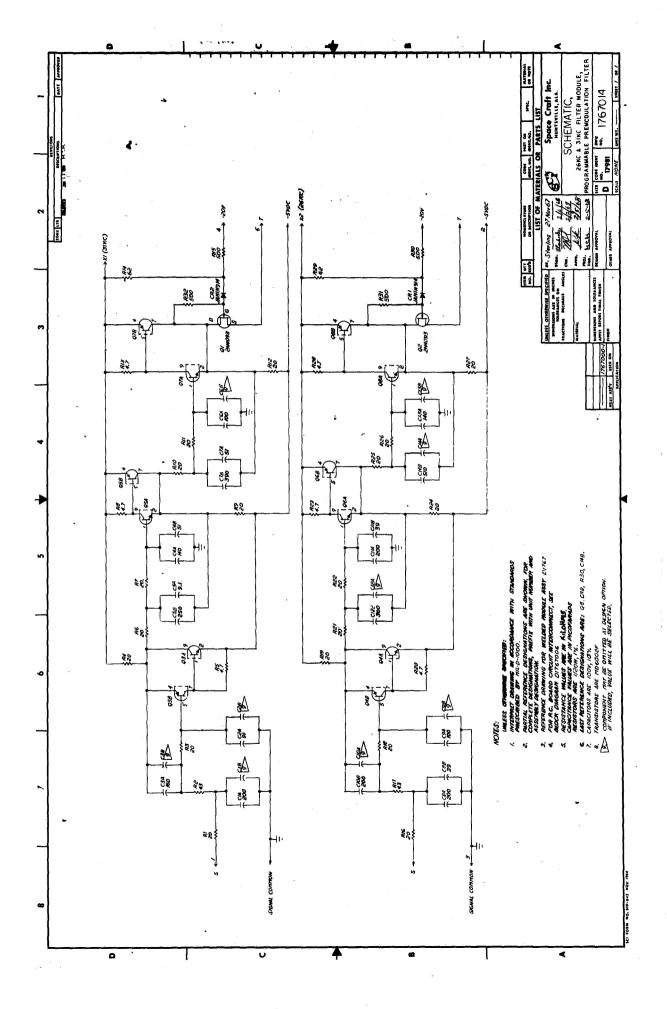


#### Filters

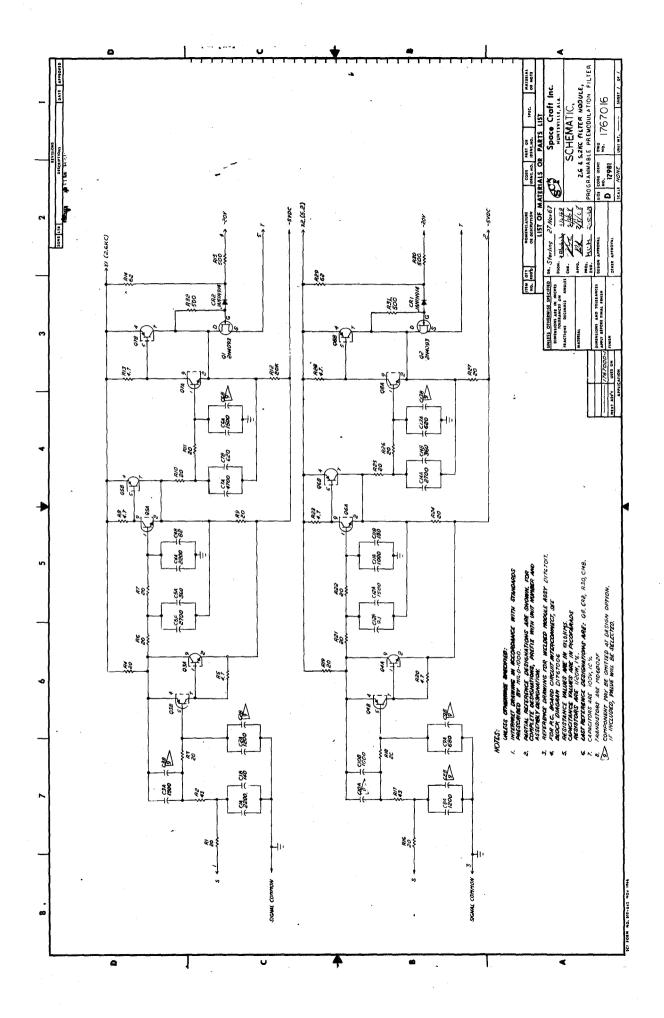
The filters are shown in Figures 1767012, 014, 016, 018, 020, 022, and 024. The filters have low pass characteristics defined by seventh order Bessel Polynomials. The Bessel characteristic gives the best reproduction of the band pass information, while holding the step response overshoot to a minimum. The filter consists of three cascaded stages to give the overall characteristic desired. The first stage is a third order section, followed by two second order sections. The filter was increased from the sixth order in the proposal to a seventh order to obtain a faster roll-off near the corner frequency and final attenuation greater than 36 db/octave. The active elements are complementary transistors connected for unity gain to minimize the effects of transistor gain variations and output impedance on the filter characteristic.

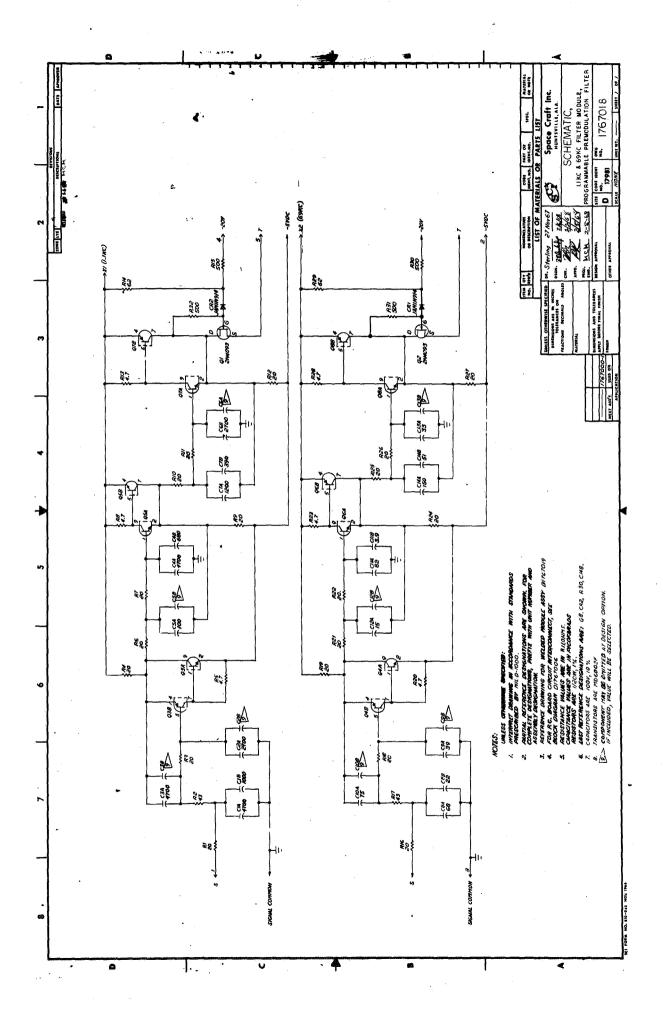
The field effect transistor connected in series with the filter output is a switch which is normally biased "off". The field effect is turned "on" when a positive twenty volts signal puts that particular filter in operation. The twenty volt filter voltage is supplied by the logic decoding circuits. The field effect transistor connects the filter to the output buffer.

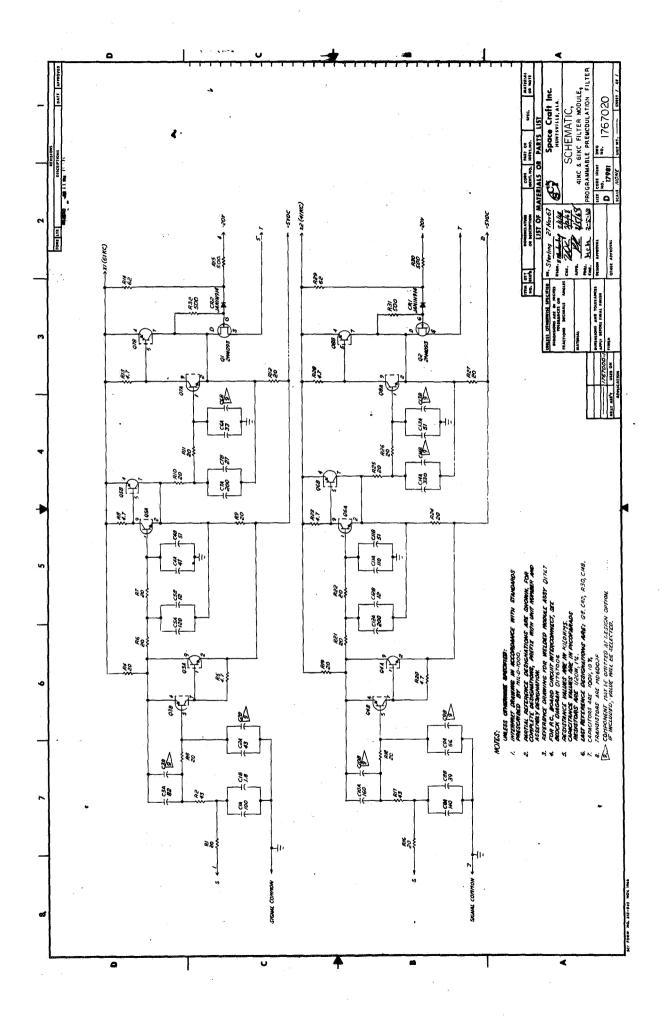


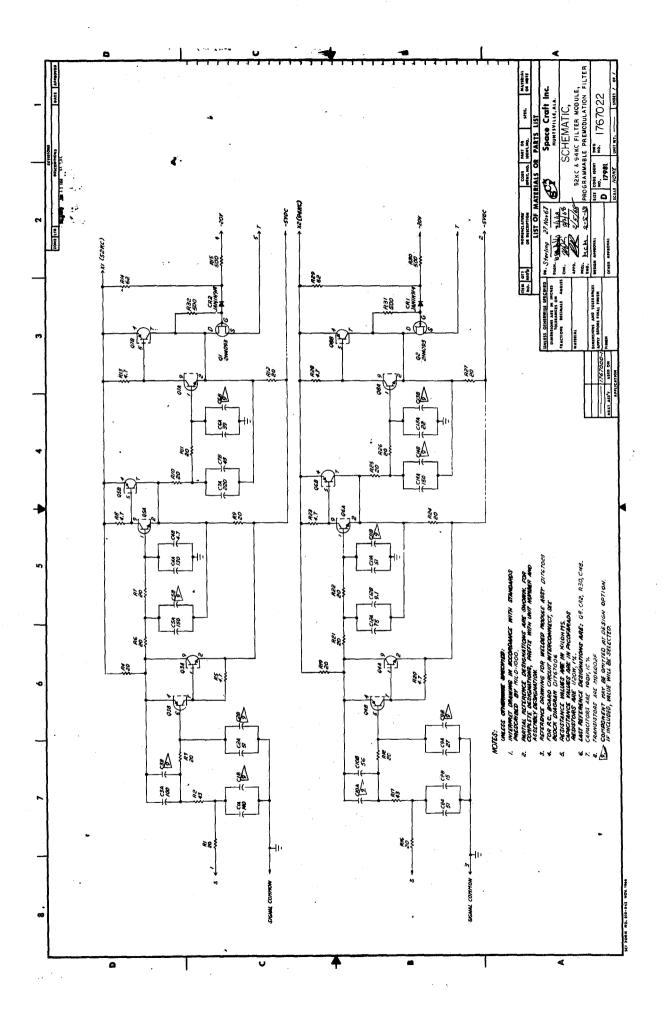


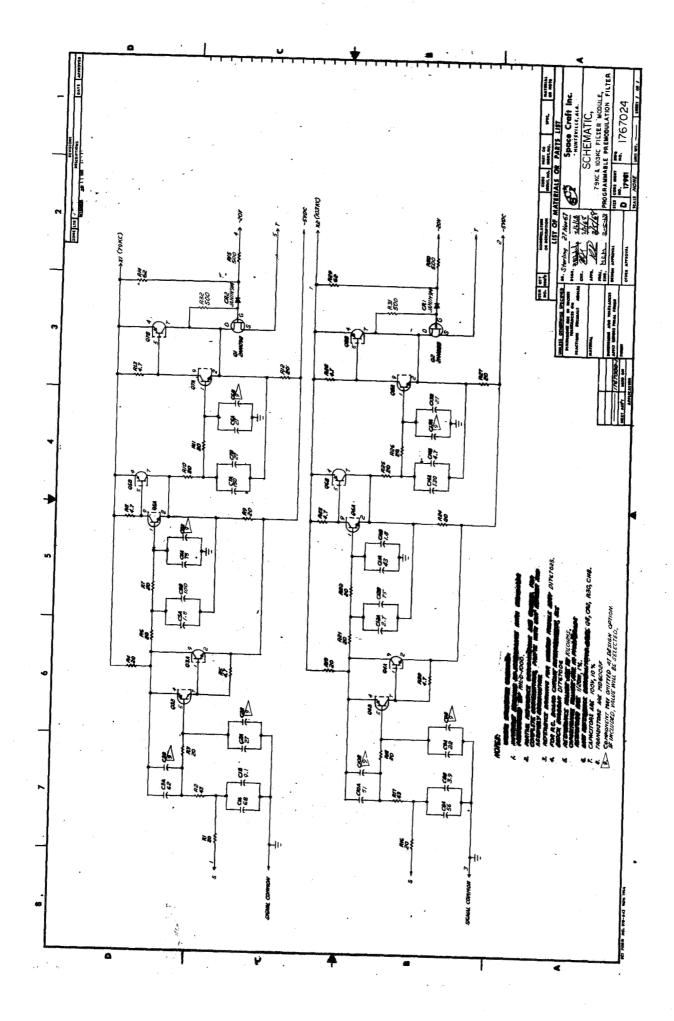
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## Output Buffer

The output buffer is shown in Figure 1767034. The circuit is identical to the output buffer used on the previous design and included in SCI proposal P67-116. Output number one produces an output of 3 volts RMS balanced about ground. The nominal values of the resistors are welded into the module except for  $R_9$  and  $R_6$ . The value of  $R_9$  and  $R_6$  are selected during test to obtain the desired peak to peak output voltage. The option of selecting the other resistor values was desired in case a more precision adjustment is necessary. Diode  $C_{r2}$  compensates for the  $V_{be}$  temperature drift of  $Q_{1b}$ .

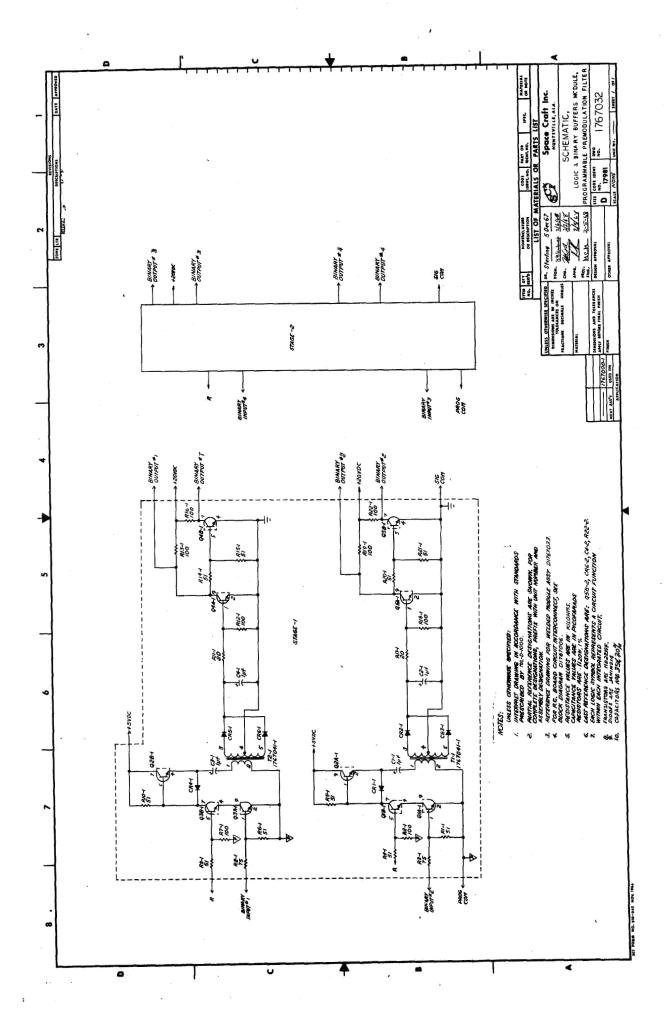
Output number two produces unipolar output from ground to five volts. The transistors are connected for unity gain. The output amplitude is fixed with the input divider chain. The  $V_{\mbox{be}}$  temperature variations are compensated for with diode  $\mbox{CR}_1$ .

# Binary Buffer

The binary buffers are shown in figure 1767032. The buffers were added to the logic circuits at the request of MSC to provide D. C. isolation between the binary inputs and all other ground systems. The input impedance is guaranteed with the 75K resistor in series with each binary input. The input transistor turns "on" a chopper which A. C. couples a signal to the logic decoding circuits. The isolated signal is processed to obtain both logic states.

## Logic Decoding

The logic decoding shown in figure 1767026 is identical to circuit proposed in the original proposal P67-116. The decoding is accomplished with NAND Gates sensitive to all high level inputs. The power to the filter is controlled with a series transistor  $Q_{1b}$ . The resistor  $R_5$  and  $C_1$  were added at the request of MSC for short circuit protection on the individual filters. The

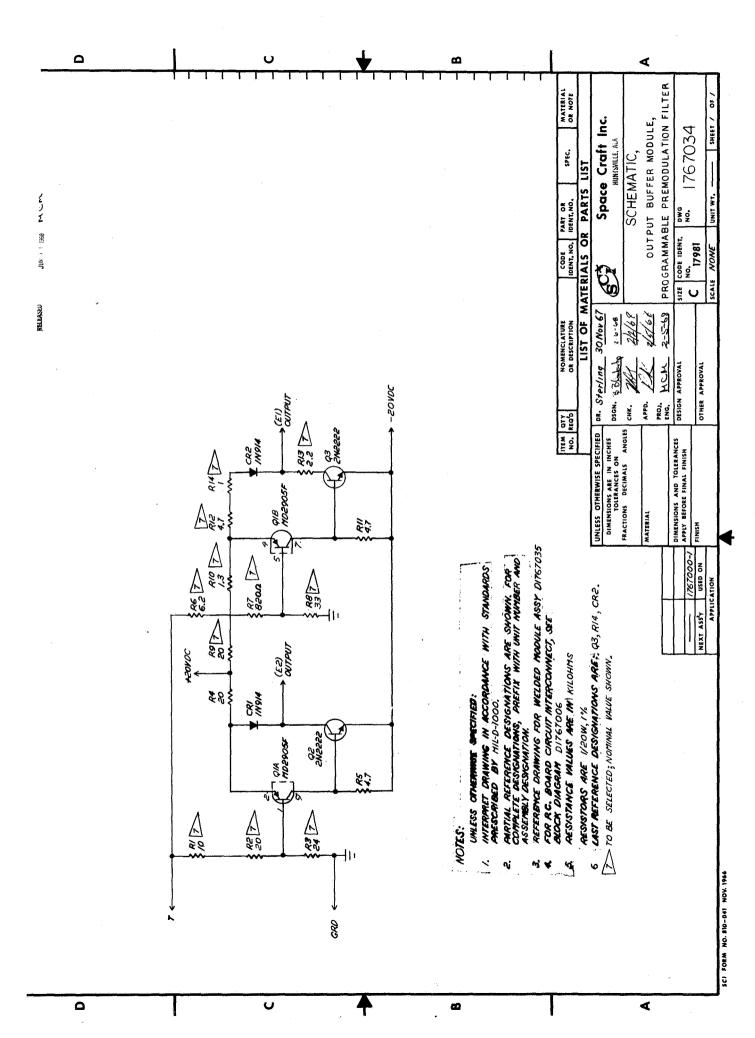


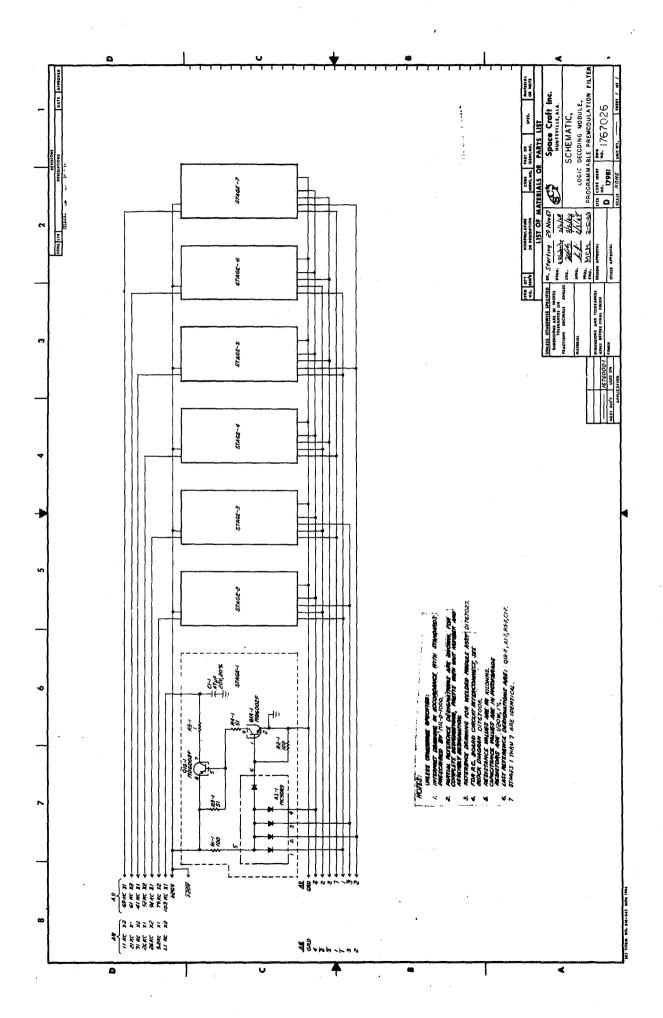
### ENGINEERING EVALUATION UNIT

The engineering evaluation unit was manufactured to verify the electrical and mechanical designs. In a high density system with the complexity of the Programmable Premodulation Filter it is desirable to evaluate a unit in the packaged configuration before producing flight units. The majority of corrections and modification involved changes to documentation.

The testing of the evaluation unit revealed several desirable modifications involving the circuit design and layout. The major change was the elimination of the printed wiring cable on the signal and power input cable. The fast rise and fall times of the signal input were capacitively coupled directly to the output through the printed wiring cable and the P. C. board track. The modification requires wiring the connector with shielded cables to the output pins on the modules. This process reduced the pickup to an acceptable level.

After all desirable modifications were made on the evaluation unit the system performance was evaluated over the required temperature range. The performance over the temperature range was excellent indicating the design and modifications were acceptable for the manufacturing of the flight systems.





protection has value in that if a filter developes a short circuit the current increase will be limited by R<sub>5</sub> to a level below the short circuit current of the power converter, thereby eliminating any possibility of a low voltage blocking condition occurring. The blocking condition is a possible result if the voltages dropped to a point that it was not possible to change from the affected filter by changing the binary code.

#### MECHANICAL DESIGN

The mechanical design proposed for the Programmable Premodulation Filter was followed in the actual design. The construction centers around microminature components welded on cordwood modules. The modules are mounted on P. C. boards and placed in an aluminum housing. The P. C. boards and modules within the housing are encapsulated with a thermal bonding foam to give maximum mechanical strength.

The only deviation from the proposal is an increase in volume resulting from the MSC requirement for D. C. isolation of the binary inputs. The volume excluding connectors is fifteen (15) cubic inches and weighs approximately 15 ounces.

## TYPE QUALIFICATION TESTING

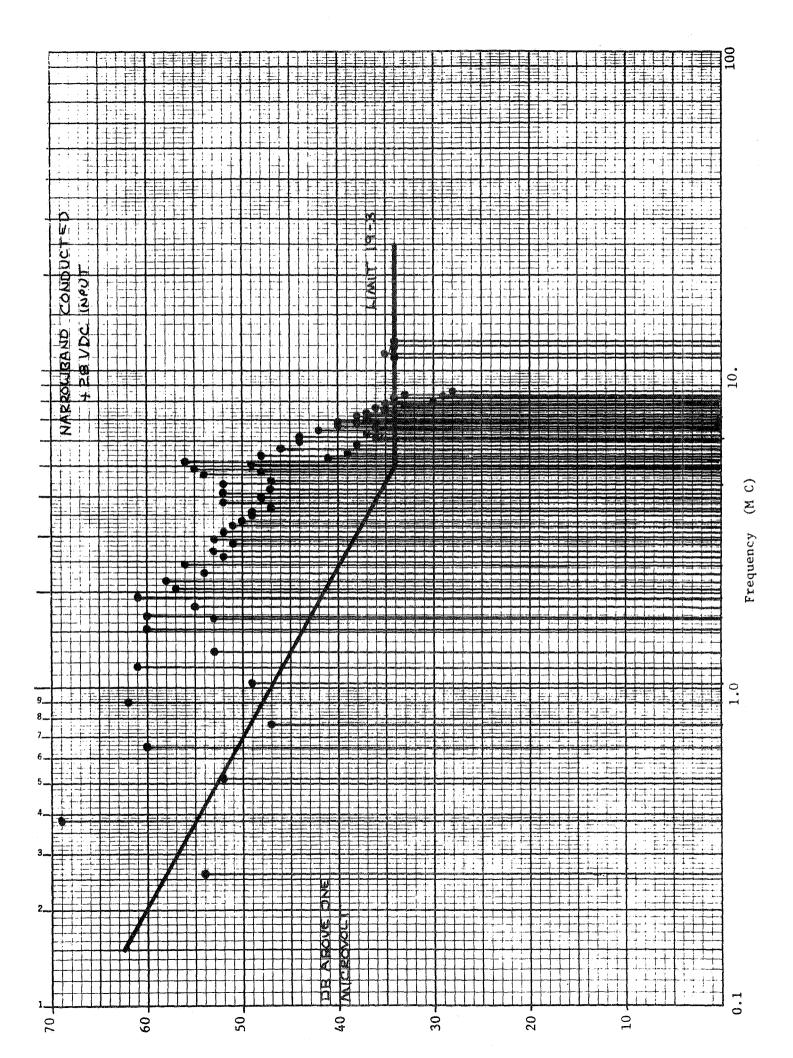
The Type Qualification Testing was performed by Space Craft, Inc. and Wyle Laboratories on the first production system. The system was tested in accordance with the SCI QTP 1767, Revision B. The particular environments provided by Space Craft were the vibration and the five day temperature cycle. The environments provided by Wyle included shock, acceleration, acoustic noise, humidity, sand and dust, altitude, deep space, thermal vacuum, explosive atmosphere, and salt fog.

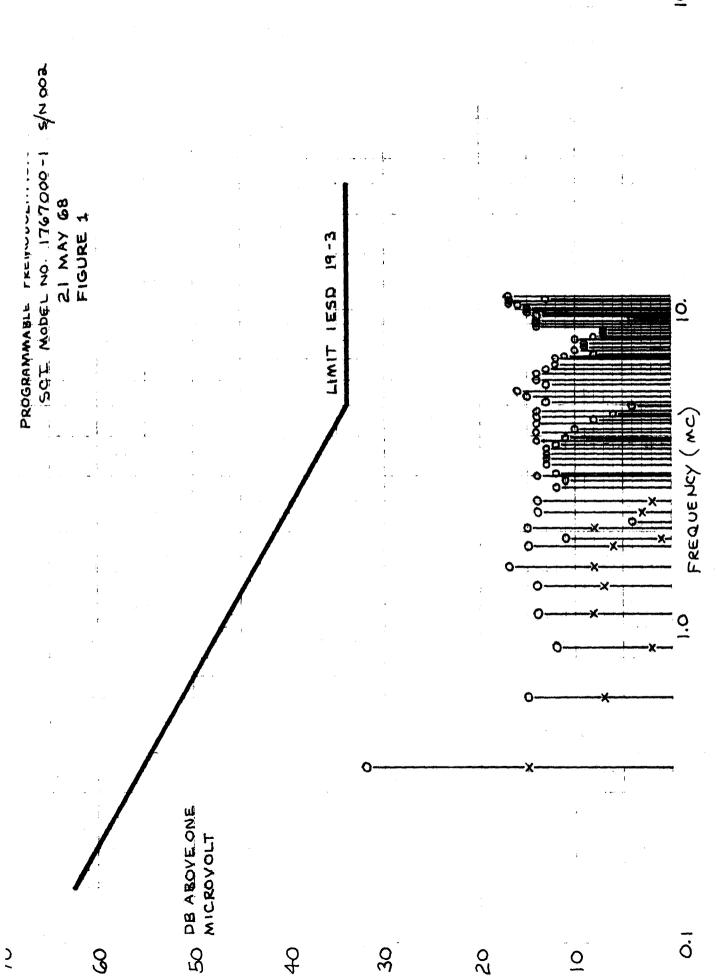
Only two failures occurred during the qualification testing. One failure was output number two went open circuit while output number one continued to function normally during the last minutes of the vibration testing. The fault was found to be the connection of the shielded cable to the rear of the connector. The connection was repaired and the area ruggedized with an adhesive. The documentation was modified to incorporate this addition.

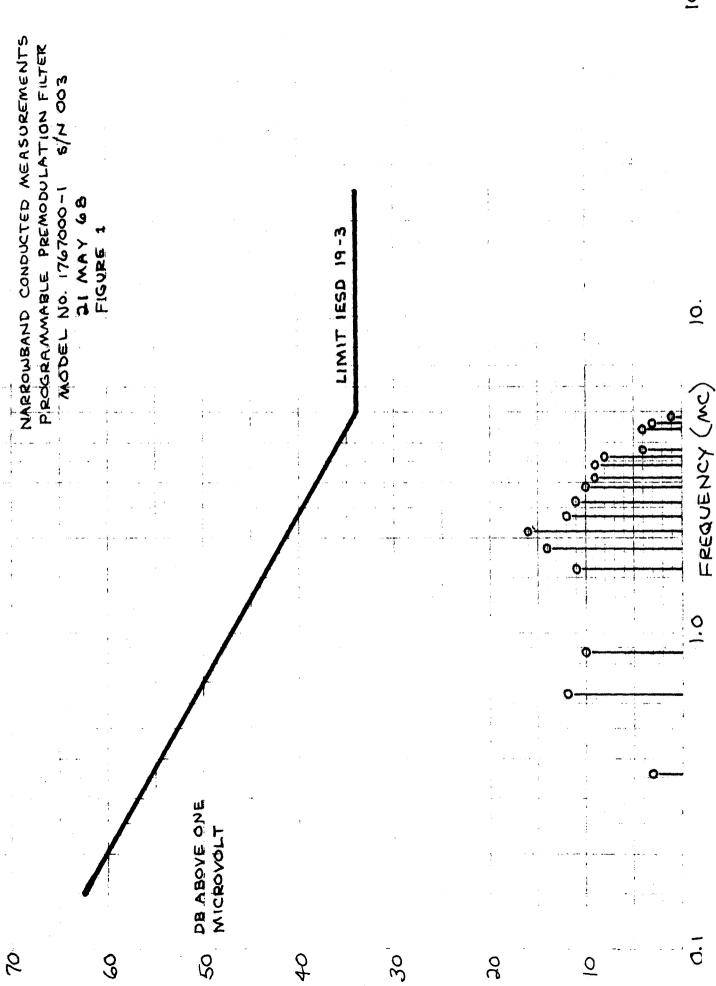
The system was reassembled and subjected to the complete vibration test again at the direction of MSC Quality Control. The total vibration time for the Qualification Unit is approximately three hours.

The other failure occurred during the RFI Test. The unit exceed the allowable limits for conducted interference of IESD 19-3. At the direction of MSC the unit was opened and modified to reduce the conducted interference to an acceptable level.

The modification consisted of increasing the values of chokes and capacitors in the power input filter and the addition of a choke in the positive 28 volt line and a choke in the power return line. Test results before and after modification are enclosed for review.







### FLIGHT QUALIFICATION

The Flight Qualification Testing was performed on the two flight system.

The Flight Qualification Testing environments included vibration, acceleration, altitude and a temperature cycle test.

The time required to perform the functional test during vibration and acceleration is approximately one and one half hours for each test. The Space Craft resident authority on environmental testing felt that such test durations might jeopardize the acceptability of the units as flight hardware. Space Craft informed MSC of the length of the present functional test and suggested an abbreviated test to reduce the vibration time. MSC directed Space Craft to test the flight units in accordance with the established functional test.

#### OPERATING INSTRUCTIONS

The Programmable Premodulation Filter power input is applied with positive twenty-eight (+28) volts to pin 15 on J1 and power common connected to pin 16 on J1. The signal input is pin 13 on J1. The input signal common is pin 11 on J1. The input signal should be 4.0 volts to 7.0 volts in amplitude with rise and fall times of 1.0 microsecond or less.

The output signal is obtained from one or both output pins. Output No. 1 is pin 18 on Jl and output No. 2 is pin 19 on Jl with signal output common on pin 8 of Jl. The output impedance is less than 1K ohms for each output.

The binary inputs are on J2 with provisions for programming the filter with a voltage provided on Pins 4 and 14 of J2. Binary one is pin 12 and 13, Binary two is pin 5 and 15, binary three is pin 3 and 11 and binary four is pin 6 and 16. To program the filter from an external source, connect a positive three to ten volts to the binary inputs for the desired binary number and the source common to pin 1, 7 or 19 on J2. To program the filter with the internal voltage, connect the voltage on pins 4 and 14 to the binary inputs for the desired binary number.

The ground systems for the internal voltage and the binary inputs are common, therefore no external connection is required for the ground systems.

The binary numbers and the corresponding cut off bit rate are listed below.

CODE	BIT RATE
0000	No Filter
0001	103 KHZ
0010	94 KHZ
0011	79 KHZ
0100	69 KHZ
0101	61 KHZ
0110	52 KHZ
0111	41 KHZ
1000	31 KHZ
1001	26 KHZ
1010	21 KHZ
1011	11 KHZ
1100	5.2 KHZ
1101	2.6 KHZ
1110	1.1 KHZ
1111	No Filter

For more detailed procedure to verify performance of the PPF or to operate the unit alone, refer to SCI ATP 1767, Revision B.

#### CONCLUSION

The design and manufacture of the Programmable Premodulation Filter proceeded with relatively few problems. The basic design of the previous Premodulation Filter Program was employed on the Programmable Premodulation Filter Program with no changes in the design philosophy. The programming capability is an addition to the past requirements. The circuit performance was satisfactory with only a few component value changes to improve the high frequency response. An improvement was incorporated into the filter sections to provide a sharper roll-off past the corner frequency which was a change from a sixth order filter to a seventh order filter.

The successful completion of the qualification testing allows significant confidence in the circuit design and reliability of the Programmable Premodulation Filter under all environments. The basic approach to active filter design as used by SCI of calculating component ratios to set filter Q values as opposed to the more common feedback gain adjustment is considered well proven and the stability exhibited by these filters over the long test period was considered very satisfactory.

The qualification testing required significantly more test time than was originally anticipated for the contract. The lengthy test time was due to the length of the functional test. This in turn was due to some extent to checking filter performance with a 10% duty cycle square wave. A sinusoidal test would be easier and quicker to perform but is not possible with the square wave buffer input. In the event of further or similar development a test point should be considered which would allow sinusoidal checking of the filters after the buffer, with a separate buffer check.

The 10% duty cycle test duration for vibration and acceleration is more than fifteen times greater than the test times in the original specification, which might suggest that the acceptability of the flight units for "flight hardware" could be jeopardized. An abbreviated test could reduce the test time and still verify the unit performance without jeopardizing the "flight hardware". Also the adoption of a sinusoidal test as suggested would simplify the problem.

Outside finish on the case survived the environmental test very well with some minor pitting in the plate after the salt fog test. Some scratching due to handling had occurred in previous tests and the scratches in the plate are considered to be the cause of the pitting.

Of the connectors used one was gold plated and the other tin plated. The tin plate was more affected by the environments than the gold plate. Gold plate was used on all flight unit connectors.

The manufacturing processes involved in the unit were standard SCI processes and no manufacturing problems encountered. It is concluded that as a result of the design and test programs the design of the unit meets all of the specification requirements and it is a manufacturable unit.